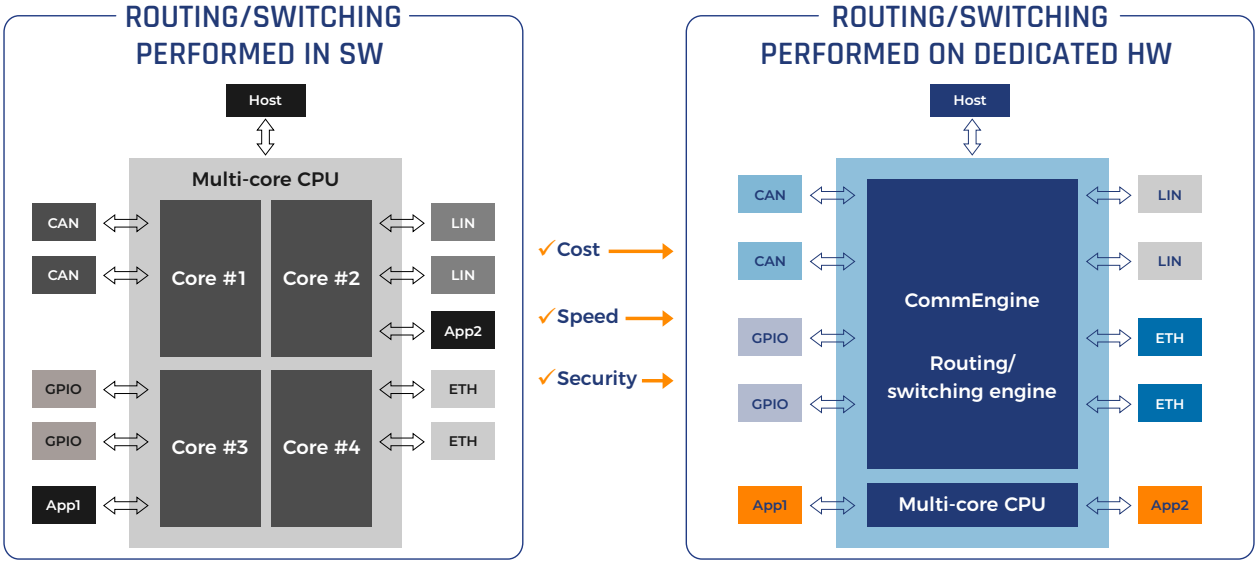
GUARDKNOX COMMENGINE™

GUARD KNOX

INTRO

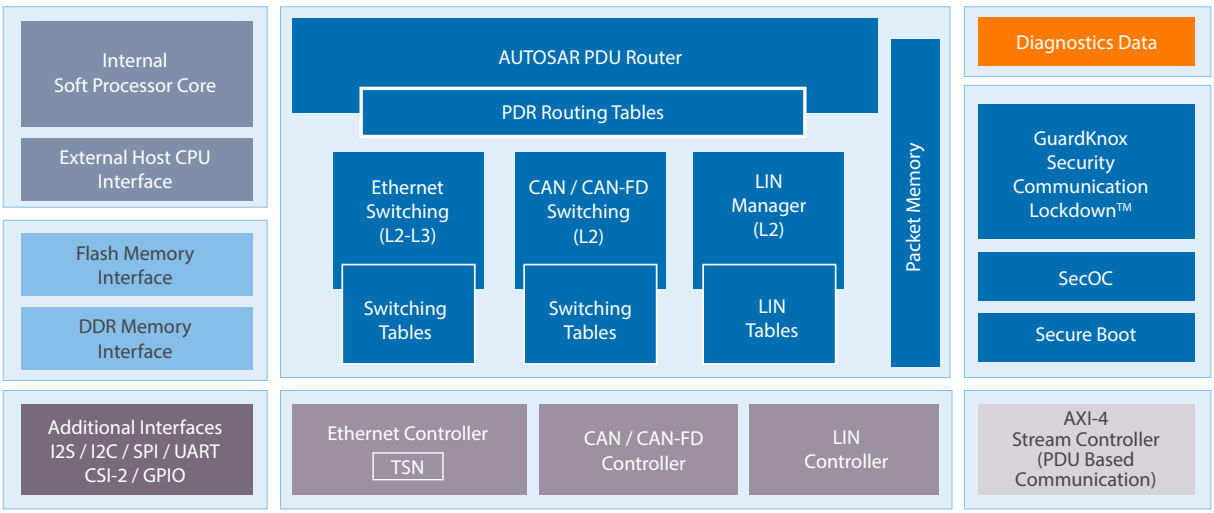
GuardKnox CommEngine™ is a single-chip solution that implements Zonal Gateway functionality and enables secure, high-performance and cost-effective data routing. It is also available as a highly integrated IP Core, running on any suitable target FPGA or ASIC. The secure-by-design routing technology allows deterministic ultra-low latency with multi-gigabit bandwidth implemented in hardware to enable next generation automotive E/E architectures.



* This configuration can be built-to-spec or customized according to technical requirements

KEY FEATURES

- Enables switching and routing of common automotive protocols (CAN, CAN-FD CAN-XL, LIN, ETH, including L5 AUTOSAR PDU Router)
- Interfaces with FPGA/ASIC internal logic (external to the CommEngine) through AXI-4 stream standard interface
- Flexible solution with configurable routing tables created by an offline tool (created from ARXML or other formats)
- Real-time bit-level, deep-packet and context-based communication inspection/verification, firewall features, and encryption acceleration implemented in HW
- Up to 10Gbit/s of bandwidth – including TSN support
- Custom interfaces supported - e.g. digital sensor interfaces, analog sensor interfaces, SPI, I2C, etc.
- Flexibility of implementing either as FPGA or ASIC
- Supports communication with external µP/µC



PRODUCT USE CASES

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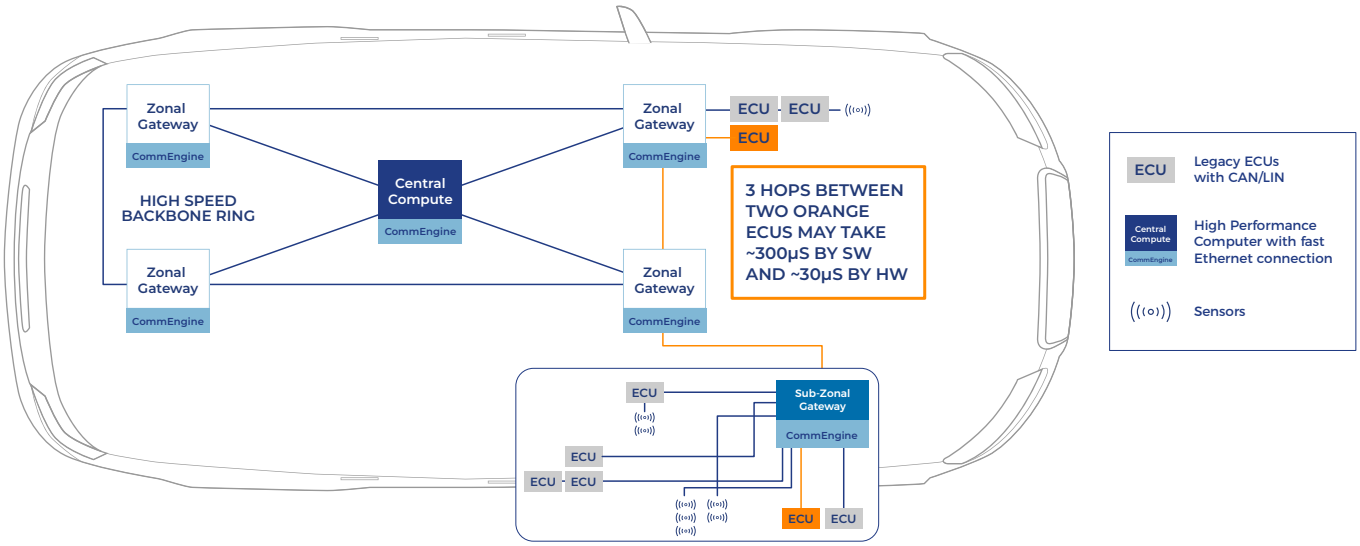
Interfaces and cores could be added or removed per demand:

HPC connectivity – CommEngine™ integrated in HPC (High Performance Compute) for interconnection of high-bandwidth backbone and external sensors, ECUs and Gateways.

Zonal Gateway – CommEngine™ implementation targeted at Zonal Gateway application and used for routing between low-speed and high-speed interfaces, PDU construction and reconstruction, streaming, security, and multi-gigabit switching. Additional computation cores MCU/CPU/GPU/NPU can be added or removed according to specific applications' acceleration needs.

Sub-Zonal Gateway – CommEngine™ implementation targeted at localized aggregation of low bandwidth interfaces (CAN, LIN, sensors, I/O) into a single high bandwidth upstream interface (Ethernet) such as a sub-zonal door module.



KEY BENEFITS

- **Guaranteed throughput with deterministic latency -** Latency reduction for routing/switching by a factor of up to 10x through massive parallelization. Even functionality with deterministic low latency requirements can now be confidently routed via zonal gateways with guaranteed throughput.
- **Reduced cost with improved performance -** Integration into one chip or IP core reduces the number of required IC's and therefore reduces the cost significantly without limiting scalability and functionality. No time-consuming and complex vehicle network optimizations are required for deployment.
- **Increased flexibility -** Increased flexibility (e.g., ports, protocols) in early stages through FPGA implementation with no need for long and complex redevelopments (e.g., switch to another MCU/MPU platform). Additionally routing tables can be easily updated via ARXML upload
- **Straightforward transition -** Completely synthesizable to any ASIC or FPGA technology per vehicle requirements.

Contact us at info@guardknox.com to learn more